IN THE CLAIMS:

1. (Currently Amended) For use in a wide-issue pipelined processor, a mechanism for reducing pipeline stalls between conditional branches, comprising:

a mispredict program counter (PC) generator that generates a mispredict PC value for each conditional branch instruction in a pipeline of said processor; and

mispredict PC storage, coupled to said mispredict PC generator and including a mispredict PC queue and a number of staging registers, that stores said mispredict PC value at least until a resolution of said conditional branch instruction occurs and makes said mispredict PC value available to a PC of said processor if said resolution results in a mispredict condition, a mispredict ~~PC queue of said mispredict PC storage having more slots than said pipeline has stages~~ said mispredict PC queue having at least as many slots as said number of said staging registers.

2. (Original) The mechanism as recited in Claim 1 wherein said mispredict PC generator is associated with a static branch predictor of said processor.

3. (Original) The mechanism as recited in Claim 1 wherein said mispredict PC generator generates a branch prediction and said mispredict PC value in a single clock cycle.

4. (Original) The mechanism as recited in Claim 3 wherein said branch prediction is employed to prefetch instructions.

5. (Cancelled)

6. (Currently Amended) The mechanism as recited in Claim 1 wherein said mispredict PC value moves through said staging registers of said mispredict PC storage as said conditional branch instruction moves through stages in said pipeline.